Application Note AN6002

APVSG Fast Control Port

Purpose

For fast, time critical settings and data streaming the APVSG can be controlled over an external port. This application note explains the configuration and usage of the Fast Control Port.

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Introduction

The Fast Control Port (FCP) is a parallel port with the possibility for the user to control specific aspects of the APVSG. When activated, the FCP can be configured to operate in one of multiple modes. With each mode, the data streamed to the FCP interface is interpreted differently and forwarded to specific parts of the device for further utilization.

Depending on the options purchased for the APVSG, different FCP modes are supported by the device. Please consider the section *Requirements and Compatibility* for details hereto. An overview of all available [CN1]modes can be found in section *FCP Operation Modes*.

Each of the FCP modes lets the user control the modulation and/or the carrier by streaming a selection of IQ data, segment IDs or carrier settings through the FCP interface to the device, as shown in *Figure 1*.

The details to each mode, including setup information and examples can be found in the subsequent chapters that each explain one FCP mode. A full list of supported SCPI commands regarding the FCP interface is given at the end of this document.

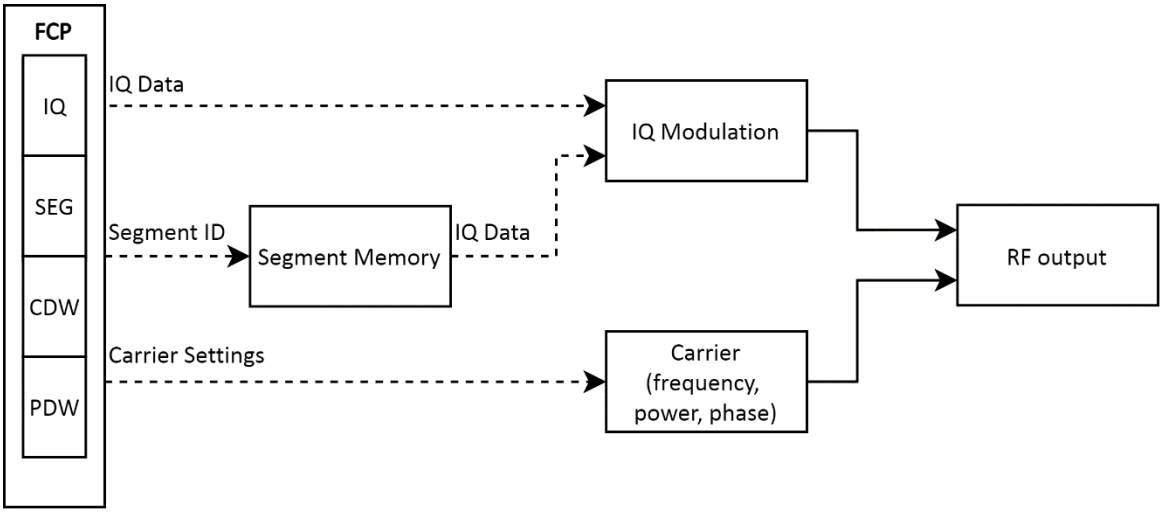


Figure 1: Functional diagram of FCP in APVSG with non-FCP parts omitted.

This document focuses on the FCP interface functionality and its settings, for further information about the specific features of the APVSG, please consult the respective Application Notes.

Interface Overview

Requirements and Compatibility

Device Options

- The FCP interface is an optional feature that can be equipped on each channel (separately) of an APVSG device at the time of ordering. The option FCP must be equipped for each channel of the device to support the FCP functionality described in this document.
- The two FCP modes, IQ Stream and Segment Stream, are both provided with the option FCP and don't require any additional options to be purchased.
- With both the FCP and UFS option, the Control Descriptor Word [CN2](CDW) feature and the FCP CDW mode are activated. They allow the user to control both the segment IDs for replayed segments, as well as basic carrier settings.
- Option PDW makes the pulse descriptor word (PDW) feature available. Combining it with option FCP activates the possibility to stream PDWs through the FCP interface in PDW mode. This feature gives the user complete control of the RF output through the FCP interface.

FCP Interface Feature

- The FCP interface is limited to only have one FCP mode active[CN3] at a time. Any active FCP mode must be disabled before a different one can be enabled.
- The FCP interface can receive 18 bits, with one clock bit, one valid bit and 16 data bits, as depicted in *Figure 2*.
- Enabling an FCP mode lets the interface receive the streamed bits and interpret them accordingly. To utilize the received data in the device, the respective feature must be enabled or set to the correct source. Information hereto can be found in the detailed description of each FCP mode.
- For the IQ Stream mode, a source-synchronous clock is required at the FCP interface. Other modes sample the streamed bits at the interface without a source-synchronous clock.
- All FCP modes require a valid signal for correct operation. Specifics for each FCP mode are given in the respective chapters.

FCP Operation Modes

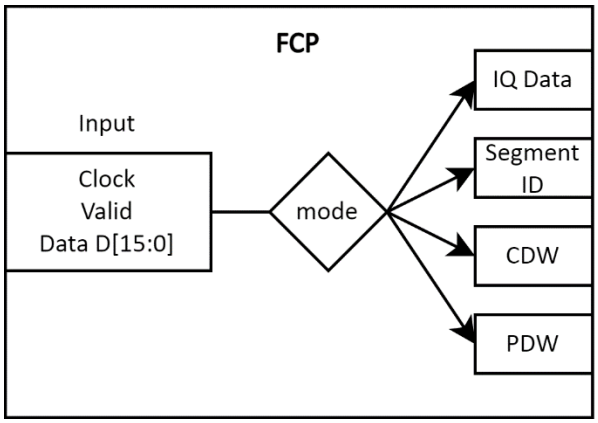


Figure 2: 18-bit FCP input being interpreted depending on the enabled FCP mode.

IQ Stream

This mode allows the user to stream IQ data to the APVSG directly and thus modulate the carrier frequency, as depicted by the “IQ Data” path directly impacting the IQ Modulation in *Figure 1*.

Segment Stream

Instead of streaming the IQ modulation data directly through the FCP, the modulation data can also be replayed from the local APVSG IQ segment memory. By streaming the memory segments IDs of the desired IQ data to the FCP, the user can directly choose the replayed segment.

CDW Stream

With the additional UFS option, the user gains access to the Control Descriptor Word (CDW) functionality of the device. It allows users to both stream segment IDs and carrier settings for a more elaborate control of the RF output.

PDW Stream

The Pulse Descriptor Word (PDW) feature, which is available as an additional option, gives the user complete control of the RF output. This feature not only provides control of segments and carrier settings, but also includes complete control of the timing at the RF output.

IQ Data Streaming with FCP

The FCP can be set as an input for IQ modulation data which is then directly applied to modulate the carrier frequency. To configure the device to receive IQ data on the FCP, the FCP must be set into IQ streaming mode and the FCP must additionally be set as the source of the IQ modulation data.

The FCP for the source-synchronously clocked IQ streaming consists of 16 IQ-data bits, a valid bit, and a clock. The clock is a continuous signal at a fixed frequency with the valid bit and IQ data transmitted in single data rate (SDR). The FCP can operate at two different playback rates, namely

- 125 Mega samples per second with a continuous 250 MHz clock
- 250 Mega samples per second with a continuous 500 MHz clock

Please note that some devices only support the 125 MSps speed option for FCP. Please check the specifications for your device or ask your AnaPico representative for details hereof.

Limitations and requirements:

- A stable frequency of 250 MHz/ 500 MHz is required on the clock pin of the FCP.
- Data at the FCP input must be streamed at 125 MSps or 250 MSps SDR.
  This is equivalent to the data bits toggling between I and Q every 4 ns/2 ns respectively. Please consult *Figure 3* for a graphical representation.
- It is recommended to operate the sender (that drives the clock and the IQ data) and your APVSG at the same reference clock to avoid undesired frequency offset effects.

IQ Stream Timing

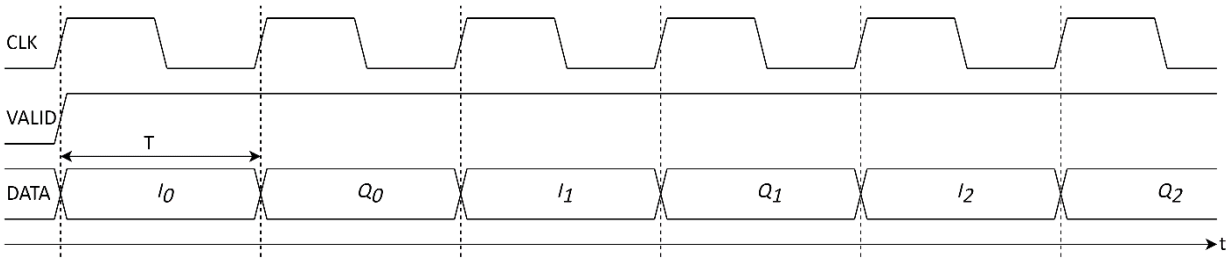


Figure 3: IQ stream input timing for the fast control port (FCP) with clock period $T \in \{2\ ns, 4\ ns\}$

The FCP receives a valid signal that is synchronized with the first valid I-data sample, followed by the first Q-data sample. The valid signal should be driven low during the setup of the device to ensure proper sampling of I and Q data samples.

The phase relationship of input signals to the FCP are depicted in *Figure 3*.See [1] for details on pin assignment at the MDR 36-pin connector.

Clock and data edges are transferred at the same time. The FCP reads the data upon each rising edge of the clock. In order to optimize and relax the sampling of the IQ data, the input delay at the FCP should be calibrated before the first IQ transmission is started. The process and requirements for calibration are explained in section *FCP Input Delay* Calibration.

Setup and SCPI Commands

Relevant SCPI commands for IQ Stream mode

A list of all FCP related SCPI commands can be found in section *SCPI Commands*.

- [:SOURce<ch>]:BB:ARBitrary:FCPort:CLOCk <freq>
- [:SOURce<ch>]:FCPort:STReam:IQ OFF|ON|0|1
- [:SOURce<ch>]:BB:ARBitrary:FCPort[:STATe] OFF|ON|0|1

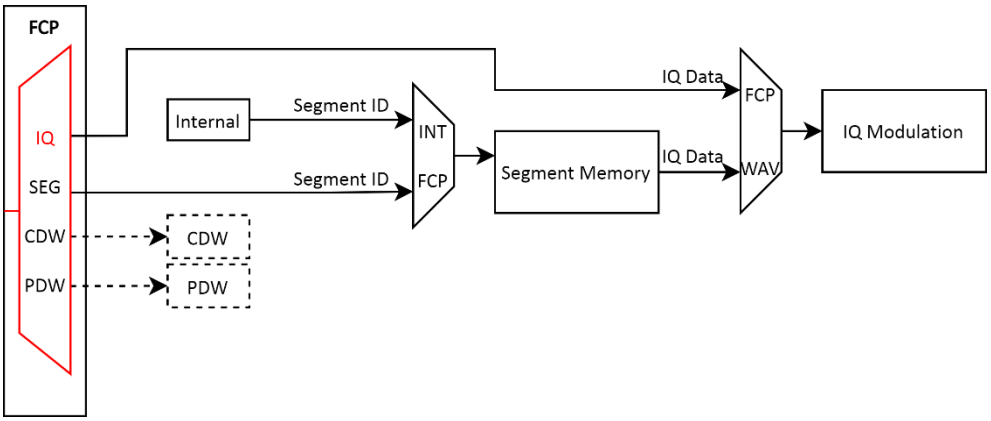


Figure 4: The FCP:STR:IQ SCPI command determines if the FCP is in IQ streaming mode. Note that this mode can only be enabled if all other FCP modes are disabled.

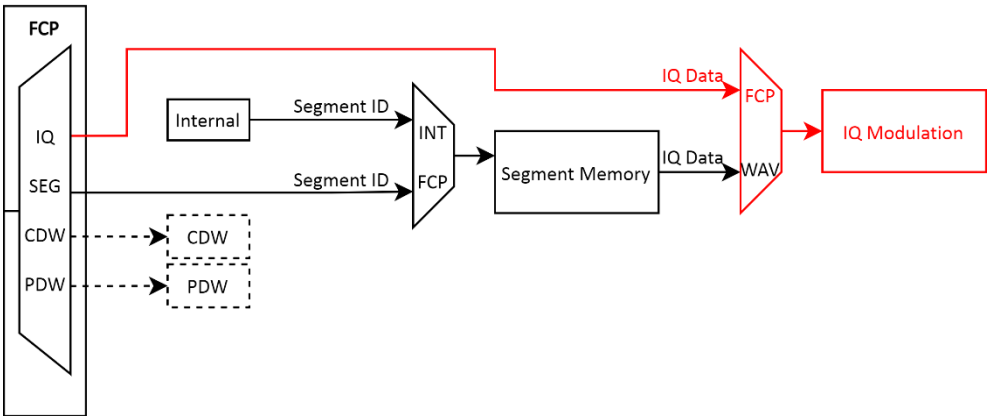


Figure 5: The BB:ARB:FCP[:STAT] command decides if the FCP IQ data is forwarded for IQ modulation. This command only takes hold if the BB:ARB:WAV:STAT command is disabled.

Configuration steps prior to transmission

1. Connect an external reference clock (recommended).
   Use the same external reference clock to drive the transmission to the FCP.
2. Connect the FCP input on the device.
3. Send a stable 125 MHz/250 MHz clock signal on the FCP connector clock pins
   (see [1] for details on pin assignment)
4. Configure the device with SCPI commands. See next section for an example.

Example

This is a SCPI example to setup the FCP interface for a single-channel device. Make sure to follow the steps prior to transmission as described in section *Setup and SCPI Commands*.

ROSC:EXT:FREQ 10e6	Sets the reference frequency to 10 MHz
ROSC:SOUR EXT	Sets the reference to external
FREQ 50e6	Sets initial RF output frequency 50 MHz
OUTP:STAT ON	Enables RF output
BB:ARB:FCP:CLOC 125e6	Sets the FCP playback rate to 125 MHz
FCP:STR:IQ ON	Sets FCP to IQ stream mode
BB:ARB:FCP ON	Sets FCP as source of the IQ modulation data

After successfully configuring the device, the IQ modulation data (e.g. a 1-tone) can be sent to the FCP - make sure the valid signal is synchronized to the first 16-bit I-data sample. A valid input IQ stream results in a modulated carrier frequency at the RF output. You can now

- Set some frequency with FREQ <x>.
- Send another IQ modulation e.g. 2-tone to the FCP input.
- Watch the output being modulated.

If you have trouble setting up the FCP to correctly receive your IQ data, have a look at section *FCP Test Mode*. The FCP IQ streaming comes with an integrated testing mode that can help detect the most common issues in your setup.

FCP Input Delay Calibration

The FCP has a built-in opportunity to calibrate the input delay for the data ports relative to the clock port. This feature allows the user to account for signal delays that occur between the different fast control port pins and thereby optimize the timing of the captured signals. This optimization is done automatically with a calibration procedure that will be explained hereafter. During the calibration process, the FCP input delay of each data bit is adjusted individually.

Step by Step Guide for Calibration

1. Start up the device
2. Physically connect an external reference clock to the APVSG device
3. Lock to the external reference
    a. SCPI commands
        ROSC:EXT:FREQ <freq> set the external reference frequency
        ROSC:SOUR EXT set the reference clock source to external
    b. or use the reference clock tab in the APVSG GUI
4. Physically connect the FCP cable
5. Send a stable input on the FCP
    a. Stable clock signal of 250 or 500 MHz depending on playback rate
    b. Keep valid signal low
    c. Data input: any arbitrary 16-bit signal
6. Configure the FCP for IQ streaming

a. SCPI commands

BB:ARB:FCP:CLOC <freq>	set the FCP playback rate (125 or 250 MHz)
BB:ARB:FCP ON	set the FCP as source for IQ modulation
FCP:STR:IQ ON	enable FCP for IQ streaming

b. Or use the APVSG GUI to set the device into FCP IQ streaming mode

7. Send the required calibration signals (see below for details) on the FCP input port
8. Start the calibration
   a. SCPI command

FCP:STR:CAL 0	start the calibration

The calibration will take several minutes to complete. Please do not modify or disturb the setup during this process.

Required Signals during Calibration

The same LFSR pattern that is used for the FCP tests is also deployed for the calibration (see section *FCP IQ Stream in Test Mode* for related information). To calibrate the FCP input with your existing setup, please make sure you meet the following requirements for the signals at the FCP interface.

- Stable clock on FCP clock pin
- Source synchronous transmission
- Pseudo-random pattern at IQ data pins
- Signal at valid pin toggling every 2.5-3 seconds
- Min. 200 valid-high periods
- FCP input signals use the same reference clock as the APVSG

Stable Clock

The input signal of the clock pin needs to be a stable 250 MHz or 500 MHz, depending on which playback you are intending to use the FCP with. If you would like to use both the 125 MSps and the 250 MSps playback rates, please either do a new calibration whenever you switch the playback rate or calibrate your FCP input with the faster playback rate.
You need to drive

- A stable 250 MHz at the clock pin for FCP with 125 MSps playback rate or
- A stable 500 MHz at the clock pin for FCP with 250 MSps playback rate.

For a proper calibration setup, please make sure the clock signal on the FCP input is generated with the same reference clock as the reference clock for the APVSG. Using an external reference clock is always recommended for streaming IQ data to the FCP.

Pattern for IQ Data

The IQ data pins of the FCP need to be driven with a predefined pseudo random pattern. See [1] for information on pin assignment on the fast control port.

The required I and Q data pattern can be generated with linear feedback shift registers (LFSR). The following code example describes how the I and Q data are generated.

```
// initialize I and Q
```

```
i_0 = 0x306C;
q_0 = 0xFFFF;
do { // for each iteration.
    i = i XOR (i << 7);
    i = i XOR (i >> 9);
    i = i XOR (i << 8);
    q = q XOR (q << 7);
    q = q XOR (q >> 9);
    q = q XOR (q << 8);
}
```

- For calibration with a 125 MSps playback rate, the I and Q data samples are sent alternatingly, with each new IQ pair representing a new iteration in the above code example. This will result in a pattern like

  ```
  i_0 = x306C     q_0 = xFFFF
  i_1 = x696F     q_1 = x7F7F
  i_2 = x5E80     q_2 = x5F9F
  ```

  and so forth. *Figure 6* depicts how the I and Q data should be sent consecutively. Please make sure there is a new data sample at every rising clock edge. The data sample that arrives along with any rising edge of the valid bit must be an I data sample – not a Q data sample. However, this data sample does not necessarily have to be the `i_0` sample. It can be any `i_n` sample if the consecutive data sample is the corresponding `q_n` sample.
- The order of I and Q samples needs to be changed slightly for calibration with a playback rate of 250 MSps. The sender must generate two pairs of IQ data samples as described in the above code example. The pairs are then sent to the FCP successively. *Figure 7* depicts the order of the required IQ data which is

  ```
  i_0 = x306C     q_0 = xFFFF     i_0 = x306C     q_0 = xFFFF
  i_1 = x696F     q_1 = x7F7F     i_1 = x696F     q_1 = x7F7F
  i_2 = x5E80     q_2 = x5F9F     i_2 = x5E80     q_2 = x5F9F
  ```

  Similar to the slower playback rate, a I data sample must be sent along with a rising edge of the valid signal.

While the valid signal is low, the 16 data pins can be driven with any arbitrary signal. The data input will thence be considered invalid and inconsequential for calibration.

Valid Signal

The signal at the valid pin of the FCP (see [1] for details on pin mapping) must stay low while the FCP is being enabled. In *Figure 6* and *Figure 7* the time periods for which the valid signal is high or low are labeled t_1 and t_2 respectively. For calibration, these periods are required to be roughly 3 seconds.

$$t_1, t_2 \in [2.3\,s, 3.5\,s]$$

For one whole calibration to finish, the valid bit must rise from low to high approximately 200 times.

Reference Clock

It is recommended to have a reference clock that drives both the APVSG as an external reference and all the signals generated by the sender of all the FCP signals. If the reference clock is not locked to both the sender and the APVSG, the FCP input calibration may fail due to frequency offset effects that cannot be circumvented.

Required FCP Signals

The following figures each show an example of the signals required at the FCP pins during calibration. All signals are explained separately and in detail in the preceding subsections.

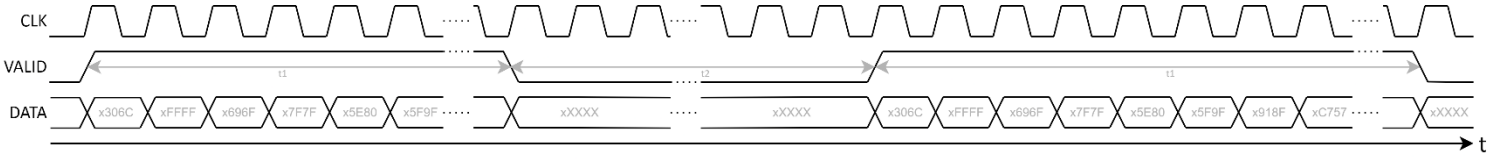


Figure 6: FCP signals for calibration with 125 MSps playback rate and 250 MHz clock. Figure not to scale.

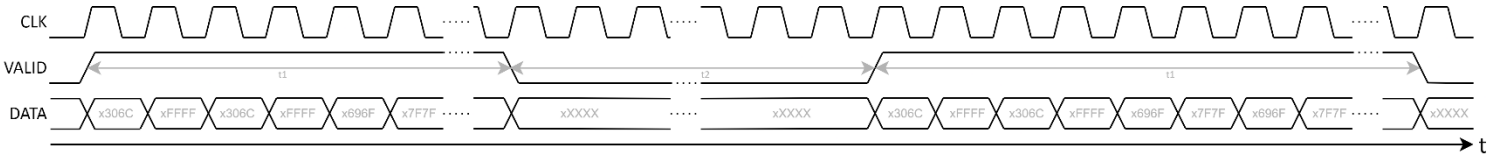


Figure 7: FCP signals for calibration with 250 MSps playback rate and 500 MHz clock. Figure not to scale.

Segment ID Streaming with FCP

The fast control port (FCP) can be configured to receive memory segment IDs to select desired memory segments for playback. When the FCP is configured in segment selection mode, the FCP cannot be configured to run in any other mode simultaneously.

The FCP expects a 16-bit wide memory segment ID, as well as a valid signal that indicates when a new ID is valid at the FCP.

Segment Stream Timing

The FCP receives a valid signal that is synchronized with the data. Each new segment ID needs to be accompanied by a rising edge of the data valid signal. The data valid[CN4] signal should be driven low during the setup of the APVSG.

The temporal relationships of the input signals to the FCP are depicted in *Figure 8.* See [1] for details on pin assignment at the connector.

Segment IDs and valid bit edges are transferred at the same time. The FCP reads the input with a sampling rate of 250 Mb per second for each signal which naturally limits the switching of the valid signal to every 4 ns the earliest.

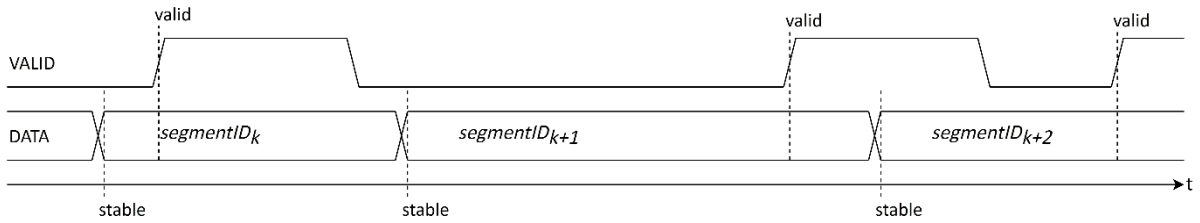


Figure 8: Timing diagram for memory segment inputs (not to scale)

Setup and SCPI Commands

Configuration steps prior to transmission

The configuration steps for segment streaming to FCP are straight forward. [CN5]

1. Connect the FCP input to the connector on the APVSG.
   See [1] for pin assignment on the FCP connector.
2. Set the FCP to Segment ID stream mode with the SCPI command
   FCP:STR:SEG ON
3. Set the segment source and enable waveform playback with SCPI commands, if desired.

Relevant SCPI commands for Segment Stream mode

A list of all FCP related SCPI commands can be found in section *SCPI Commands*.

- [:SOURce<ch>]:FCPort:STReam:SEGment OFF|ON|0|1
- [:SOURce<ch>]:BB:ARBitrary:WSEGment:SOURce INTernal|FCP|SEQuence|MF
- [:SOURce<ch>]:BB:ARBitrary:WAVe[:STATe] OFF|ON|0|1

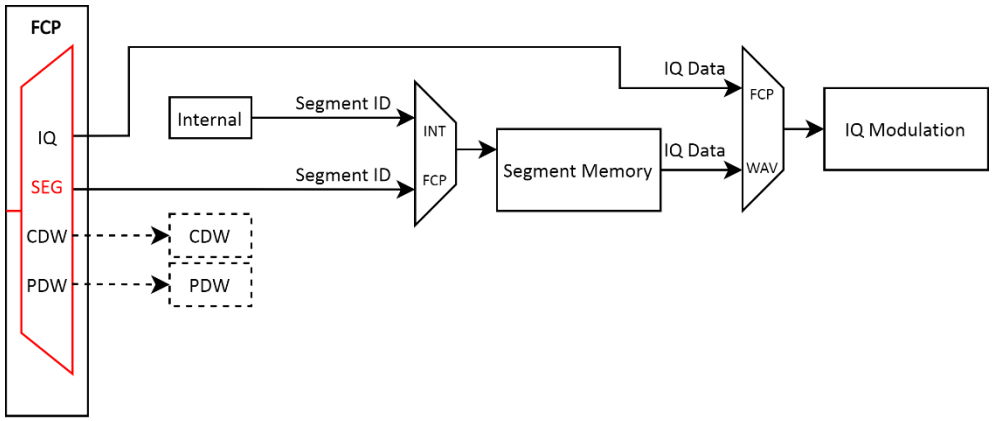


Figure 9: The FCP:STR:SEG command determines whether the FCP is streaming memory segment IDs. Note that this mode can only be enabled if all other FCP modes are disabled.

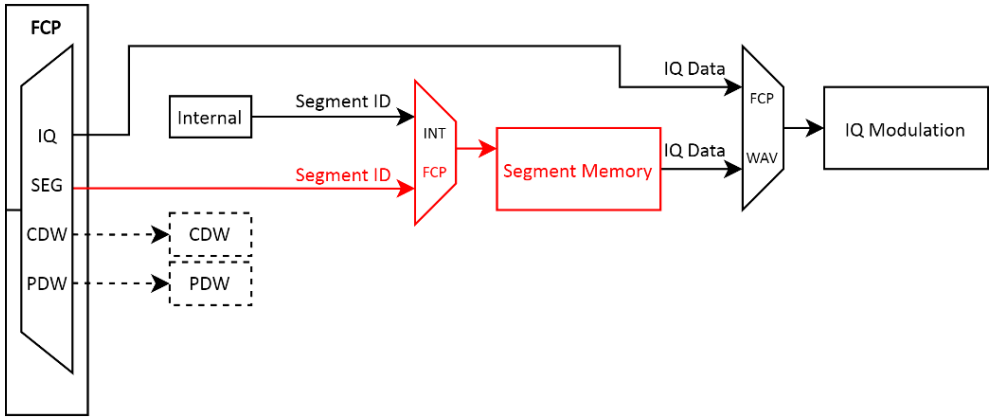


Figure 10: BB:ARB:WSEG:SOUR command sets the source for the segment ID.

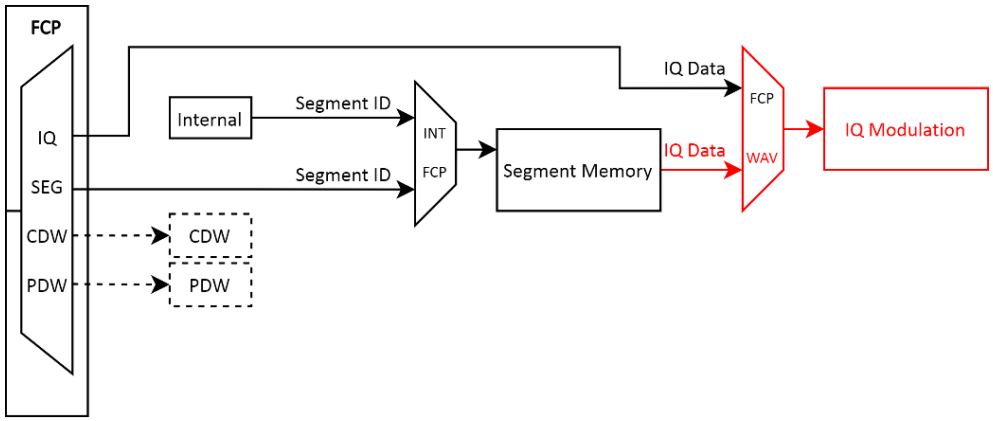


Figure 11: The BB:ARB:WAV:STAT ON command enables IQ data streaming from the selected segment in memory.

Example

1. Write some IQ data to the internal memory of the APVSG, e.g. a 1-tone modulation. This can be done by e.g. uploading the data of a QI file with the APVSG GUI.
2. You can use either the GUI or the following SCPI commands to further setup the APVSG.

FREQ 50e6	Sets initial RF output frequency 50 MHz
OUTP:STAT ON	Enables RF output
BB:ARB:WSEG:SOUR FCP	Sets FCP as source for segment selection
FCP:STR:SEG ON	Sets FCP to segment stream mode
BB:ARB:WAV:STAT ON	Sets RAM as source of the IQ modulation data

After successfully configuring the device, the segment ID can be sent to the FCP - make sure the positive edge of your valid signal is sent along with the 16-bit segment ID signal. You can now

- Set some frequency with FREQ <x> on the APVSG.
- Send a different segment ID with a new positive edge on the valid signal to switch the IQ modulation data replayed from the RAM.
  [Note: The device needs to have stored a waveform with the designated ID you are sending on FCP, or there will be no modulation waveform to be replayed.]
- Watch the output being modulated accordingly.

CDW Streaming with FCP

The APVSG supports Control Descriptor Words (CDW) that allow the user to control the carrier and active waveform segment remotely through the FCP interface. For more information on the CDW feature, please consult the respective Application Note [5]. While the FCP interface is configured in CDW Stream mode, it cannot be configured to run in any other mode simultaneously. The data bits streamed to the FCP in CDW mode must contain a pair of CDW, an 8-bit address and an 8-bit parameter. The data valid signal indicates valid data at the FCP interface input.

Signal	CDW Interpretation
Data 7:0	CDW parameter
Data 15:8	CDW address
Data Valid	CDW data valid
Clock	-

CDW Stream Timing

The FCP receives a valid signal that is synchronized with the data bits. Each new pair of addresses and parameters on the data bits must be accompanied by a rising edge of the valid signal which must arrive after the data bits are stable. The valid signal is to be driven low during the setup of the APVSG. The timing relationship of the different bits is shown in *Figure 12.*

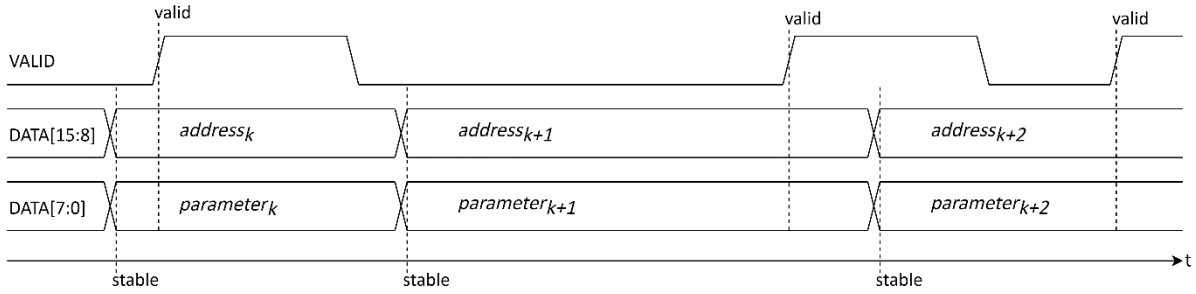


Figure 12: Timing diagram for CDW streaming (not to scale)

The FCP interface reads all input bits at a sampling rate of 250 Mb per second. This naturally limits the switching time of the valid signal to a minimum of 4ns.[CN6]

Setup and SCPI Commands

Configuration steps prior to transmission

1. Connect the FCP input at the connector on the APVSG.
   See section *FCP Connector****Fehler! Verweisquelle konnte nicht gefunden werden.*** for pin assignment details.
2. Set the FCP to CDW stream mode with the SCPI command
   FCP:STR:CDW ON
3. Set the device to CDW mode to interpret the received CDW data on FCP with
   CDW:STAT ON

Relevant SCPI commands for CDW Stream mode

A list of all FCP related SCPI commands can be found in section *SCPI Commands*.

- [:SOURce<ch>]:FCPort:CDW:STReam OFF|ON|0|1

- [:SOURce<ch>]:CDW:STATe OFF|ON|0|1

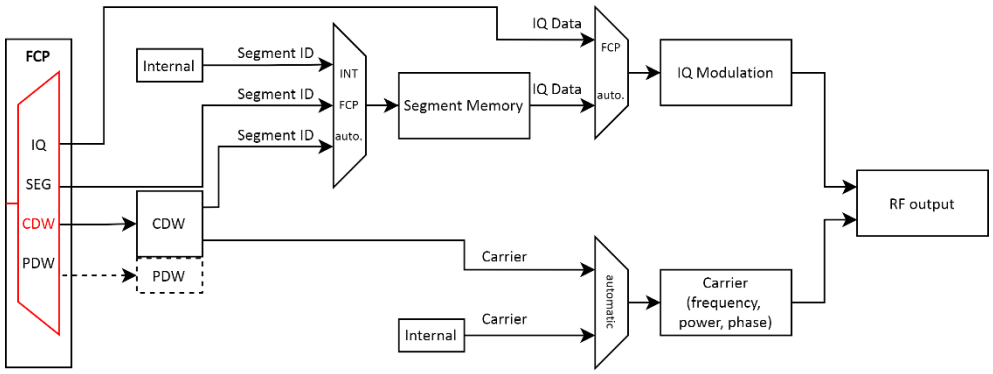


Figure 13: The FCP:STR:CDW command determines whether the FCP is streaming CDW parameters. Note that this mode can only be enabled if all other FCP modes are turned off.

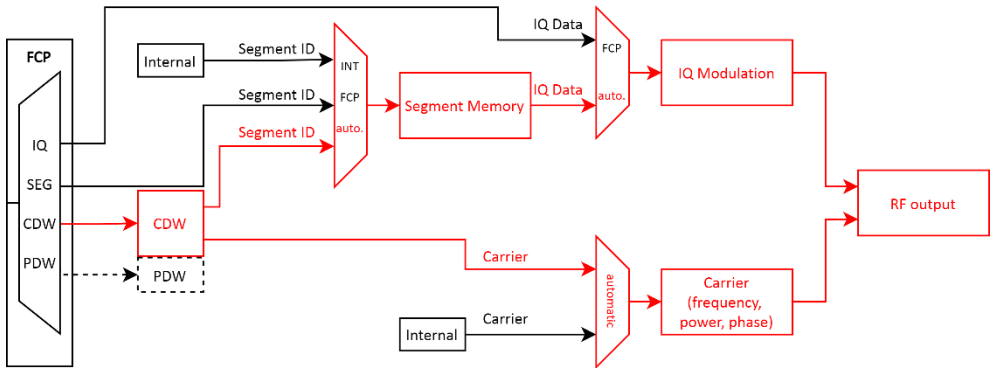


Figure 14: CDW:STAT command enables the CDW feature that takes control of te RF output.

Example

1. Connect the FCP input at the connector on the APVSG
2. Write some IQ data to the internal memory if you intend on enabling the waveform playback of a segment with CDW. This can be achieved e.g. with the APVSG GUI.
3. Configure the APVSG channel you desire to stream CDW to, with the following commands.

FCP:STR:CDW:STAT ON	Enables the CDW mode of the FCP
CDW:STAT ON	Enables the CDW subsystem.

After successfully configuring the device, pairs of CDW addresses and parameters can be transmitted to the FCP along with the valid signal as described in *CDW Stream Timing*. Please make sure to always send the CONFIG_END parameter after all necessary parameters of one CDW, as this will apply the set CDW at the RF [CN7]output. For a list of available address and parameter pairs of the CDW feature, please take a look at the respective Application Note [5].

PDW Streaming with FCP

The APVSG supports Pulse Descriptor Words (PDW) that allow the user to control the carrier and active waveform segment remotely, through the FCP interface. For more information on the PDW feature, please consult the PDW Application Note [4]. When the FCP interface is configured in PDW Stream mode, it cannot be configured to run in any other mode simultaneously. The data bits streamed to the FCP in PDW mode must contain a pair of PDW an 8-bit address and an 8-bit parameter. The valid signal indicates valid data at the FCP interface input.

Signal	PDW Interpretation
Data 7:0	PDW parameter
Data 15:8	PDW address
Data Valid	PDW data valid
Clock	-

PDW Stream Timing

The FCP receives a valid signal that is synchronized with the data bits. Each new pair of addresses and parameters on the data bits must be accompanied by a rising edge of the valid signal which must arrive after the data bits are stable. The valid signal is to be driven low during the setup of the APVSG. The timing relationship of the different bits is shown in *Figure 12*.

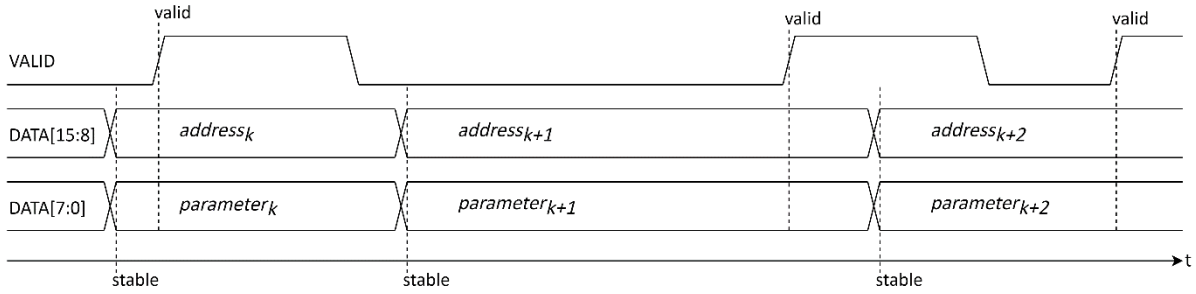


Figure 15: Timing diagram for PDW streaming (not to scale)

The FCP interface reads all input bits at a sampling rate of 250 Mb per second. This naturally limits the switching time of the valid signal to a minimum of 4ns.

Setup and SCPI Commands

Configuration steps prior to transmission

4. Connect the FCP input at the connector on the APVSG.
   See section FCP Connector for pin assignment details.
5. Set the FCP to PDW stream mode with the SCPI command
   FCP:STR:PDW ON
6. Set the device to PDW mode to interpret the received PDW data on FCP with
   PDW:STAT ON

Relevant SCPI commands for PDW Stream mode

A list of all FCP related SCPI commands can be found in section *SCPI Commands*.

- [:SOURce<ch>]:FCPort:PDW:STReam OFF|ON|0|1
- [:SOURce<ch>]:PDW:STATe OFF|ON|0|1

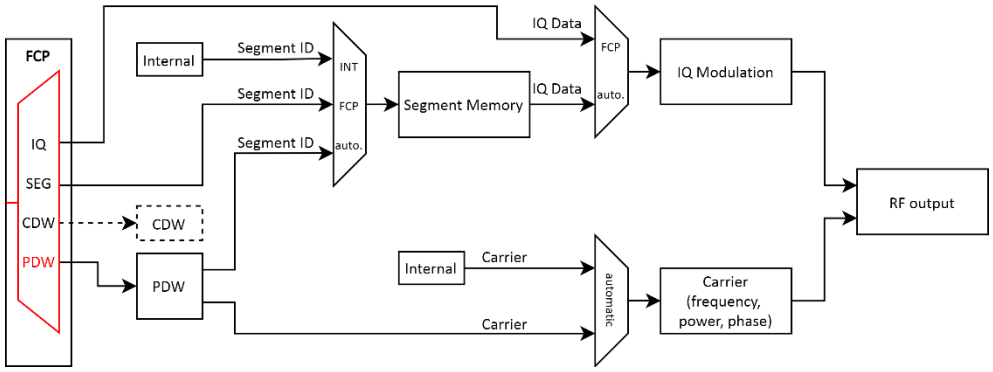


Figure 16: The FCP:STR:PDW command determines whether the FCP is streaming PDW parameters. Note that this mode can only be enabled if all other FCP modes are turned off.

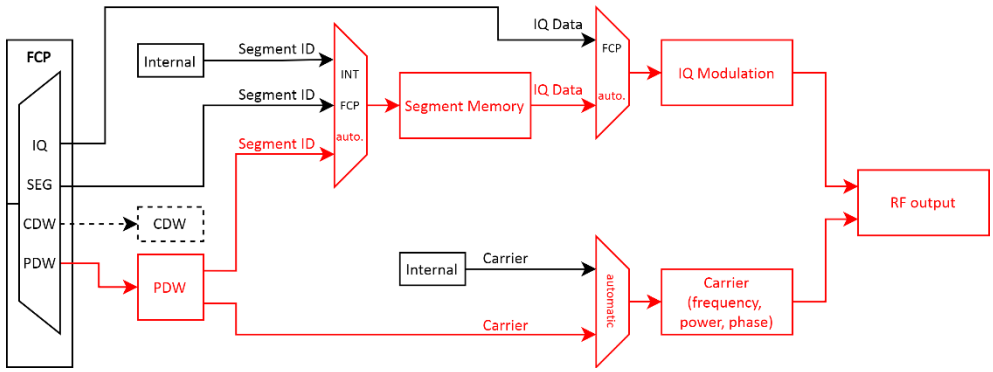


Figure 17: PDW:STAT command enables the PDW feature that takes control of te RF output.

Example

4. Connect the FCP input at the connector on the APVSG
5. Write some IQ data to the internal memory if you intend on enabling the waveform playback of a segment with PDW. This can be achieved e.g. with the APVSG GUI.
6. Configure the APVSG channel you desire to stream PDW to, with the following commands.

FCP:STR:PDW:STAT ON	Enables the PDW mode of the FCP
PDW:STAT ON	Enables the PDW subsystem.

After successfully configuring the device, pairs of PDW addresses and parameters can be transmitted to the FCP along with the valid signal as described in *PDW Stream Timing*. Please make sure to always send the CONFIG_END parameter after all necessary parameters of one PDW, so parameters are assigned to the correct PDW. For a list of address and parameter pairs of the PDW feature, please take a look at the PDW Application Note [4].

FCP Test Mode

The following sections describe the behavior of the FCP in test mode. For each streaming mode of the FCP the functionality of the test varies to account for the type of transmission employed in the specific streaming mode.

There are two SCPI commands for FCP testing. One command to enable or disable the test mode for FCP and a second command to print the related information on the active FCP streaming mode and the testing of this mode.

Related SCPI Commands

- **[SOURce<ch>:]FCPort:TEST OFF|ON|0|1**
- **[SOURce<ch>:]FCPort:DIAGnostic**
- **[SOURce<ch>:]FCPort:DIAGnostic?**

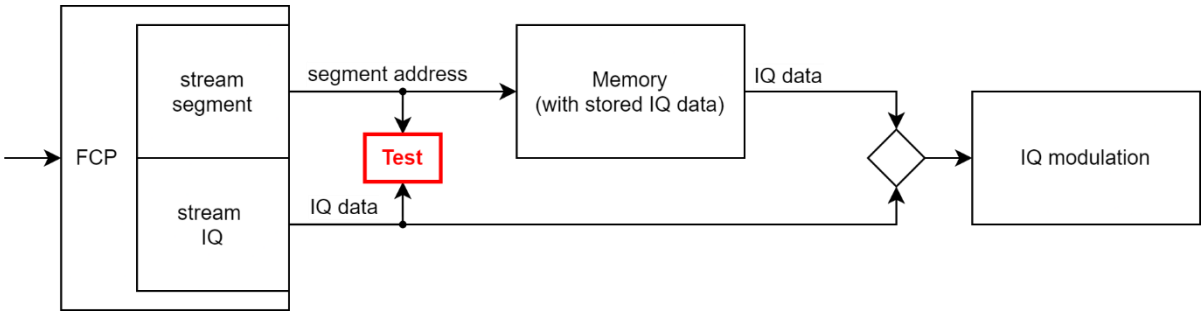


Figure 18: The FCP:TEST command dictates if the FCP is being run in test mode. Please note that the behavior of the FCP test depends on the applied streaming mode at any given time.

The displayed information varies according to streaming mode. When the FCP test mode is activated, the test information and results are show along with the diagnostic information on the current FCP state.

FCP IQ Stream in Test Mode

The diagnostic information for the FCP relays the state of the received clock on FCP. For the FCP to be able to sample the IQ data correctly in IQ streaming mode, the respective clock pin must be driven with a stable clock signal with 50% duty cycle. The FCP will only be able to lock onto the clock signal if it is stable. Consult the FCP:DIAG SCPI command to check if your applied clock signal meets these requirements. Please note, that it is recommended to drive this clock signal and the reference clock for the APVSG with the same source clock to avoid undesired frequency offset effects.

Once a sufficient clock signal is applied, the IQ data can be tested for correct transmission. The FCP IQ stream mode contains a built-in test that makes use of a linear feedback shift register (LFSR) to generate a pseudo-random test pattern for the I-data and the Q-data separately. Thus, all combinations of the 16-bit IQ data are tested except for the 0x0000 combination. In the following, the iterations to generate the test pattern are described in pseudo code.

```
// initialize I and Q
i_0 = 0x306C;
q_0 = 0xFFFF;
do { // for each iteration.
    i = i XOR (i << 7);
    i = i XOR (i >> 9);
    i = i XOR (i << 8);
    q = q XOR (q << 7);
    q = q XOR (q >> 9);
    q = q XOR (q << 8);
}
```

Which will result in:

$$\mathrm{I}_0 = 0\mathrm{x306C},\ \mathrm{Q}_0 = 0\mathrm{xFFFF},\ \mathrm{I}_1 = 0\mathrm{x696F},\ \mathrm{Q}_1 = 0\mathrm{x7F7F},\ \mathrm{I}_2 = 0\mathrm{x5E80},\ \mathrm{Q}_2 = 0\mathrm{x5F9F},\ \ldots$$

The built-in comparator will wait for the initial pattern of I_0 and Q_0 to start comparing the received data. Make sure the valid bit you send to the FCP is high during the transmission of the test patterns or the FCP will not recognize the data as valid input. Also take care to send the rising edge of the valid bit simultaneously with an I-data as described in section *IQ Stream Timing.*

The comparator will then compare the data on the FCP input while it is valid and count the numbers of errors detected for each bit. The pattern comparison will stop if the valid bit is low and resume when it is high again. The diagnostic information of the FCP that can be accessed with the FCP:DIAG command gives information on the state of the valid signal, the test comparison and the amounted errors. The displayed number of errors per bit are limited to 2^{21} and will overflow if excessed. Furthermore, the presented values do not necessarily represent an exact point in time since the error counts for the separate bits are gathered consecutively and not simultaneously.

Example of a possible FCP:DIAG response:

```
******* FCP diagnostic:
        FCP State : IQ Stream (Slave)
        FCP clock : locked and frequency OK
        FCP Data  : valid

        FCP Test  : enabled
        Test State: comparing patterns
        Current error count of each bit:
        D15:    D14:    D13:    D12:    D11:    D10:    D09:    D08:
              0       0       0       0       0       0       0       0
        ------------------------------------------------------------------
        D07:    D06:    D05:    D04:    D03:    D02:    D01:    D00:
              0       0       0       0       0       0       0       0
```

FCP Segment Stream in Test Mode

The test mode for memory segment address stream is a lot simpler than for the IQ streaming mode. Since the transmission is not source synchronous but the data is sampled at the FCP input, there is only diagnostic information about the valid bit and the received address.

In test mode, the address input is directly forwarded to the diagnostic information along with the state of the valid bit.

Example of a possible FCP:DIAG command response:

```
******* FCP diagnostic:
        FCP State : Segment Stream (Slave)
        FCP ready : 1

        FCP Test  : enabled
        FCP Data  : valid
        FCP Input : 0x0004;
```

Further Information

SCPI Commands

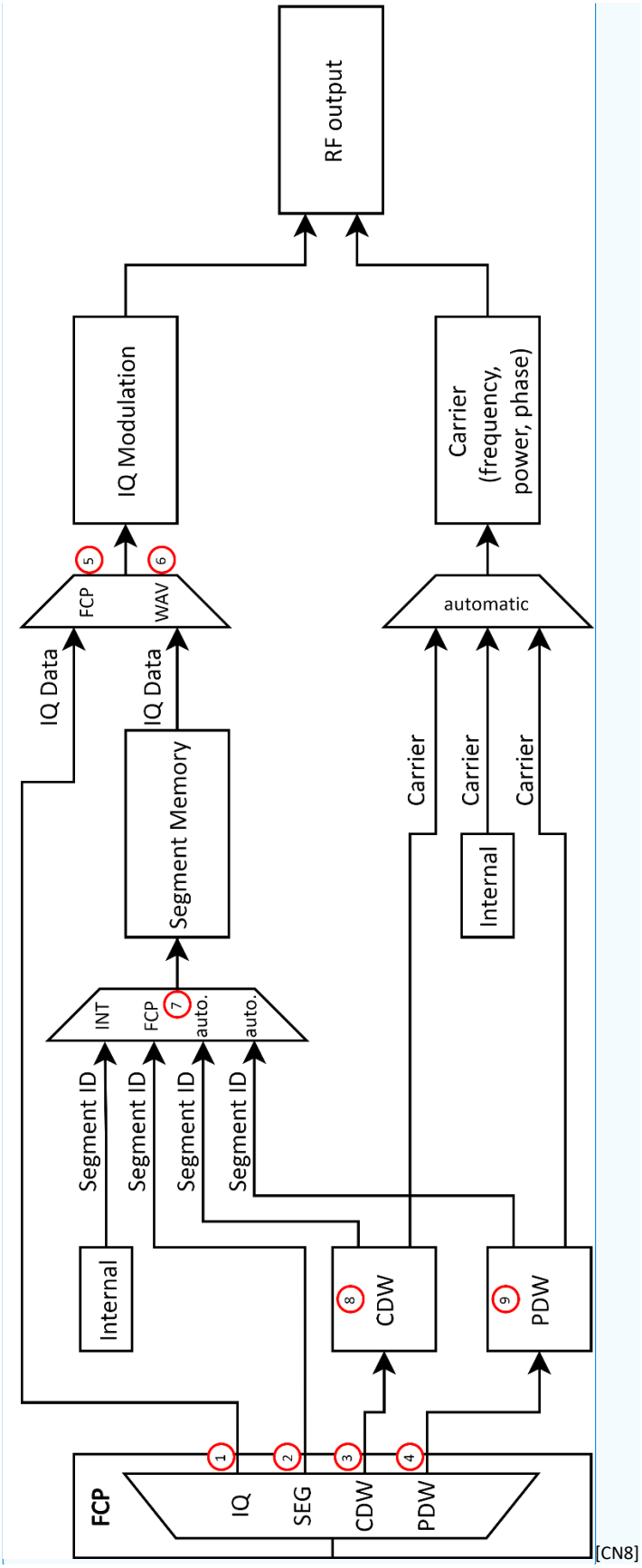


Figure 19:Overview of FCP interface and connected functionality. APVSG features not affiliated with FCP are omitted. The corresponding SCPI command for each encircled number can be found on the following pages.

This section lists all SCPI commands of the FCP feature and its related commands.

[:SOURce<ch>]:FCPort:STReam:IQ OFF|ON|0|1

1 Sets the FCP to stream IQ data.
*RST value: OFF[CN9][RE10]

[:SOURce<ch>]:FCPort:STReam:SEGment OFF|ON|0|1

2 Sets the FCP to stream segments IDs.
*RST value: OFF

[:SOURce<ch>]:FCPort:STReam:CDW OFF|ON|0|1

3 Sets the FCP to stream control descriptor words (CDWs).
*RST value: OFF

[:SOURce<ch>]:FCPort:STReam:PDW OFF|ON|0|1

4 Sets the FCP to stream pulse descriptor words (PDWs)
*RST value: OFF

[:SOURce<ch>]:FCPort:STReam:CALibrate

Runs a search to find the best input delay for the FCP interface. See section *FCP Input Delay Calibration* for details.

[:SOURce<ch>]:FCPort:TEST OFF|ON|0|1

Sets the FCP to test mode.
*RST value: OFF

[:SOURce<ch>]:FCPort:DIAGnostic

Gets diagnostic information regarding the FCP. Available for FCP in all four stream modes (IQ, SEGment, CDW and PDW)

[:SOURce<ch>]:FCPort:DIAGnostic?

Prints the previously gathered diagnostic information of the FCP.

[:SOURce<ch>]:BB:ARB:FCP:CLOC <freq>

This sets the FCP sampling and playback rate to <freq>.
*RST value: 125 MHz

[:SOURce<ch>]:BB:ARBitrary:FCP[:STATe] OFF|ON|0|1

5 Sets the FCP as the source of IQ modulation.
*RST value: OFF

[:SOURce<ch>]:BB:ARBitrary:WAVeform[:STATe] OFF|ON|0|1

6 Sets the waveform segments as the source of IQ modulation.
*RST value: OFF

[:SOURce<ch>]:BB:ARBitrary:WSEGment:SOURce INTernal|FCP|SEQuence|MF

7 Sets the segment selection source.
*RST value: INT

[:SOURce<ch>]:CDW:STATe OFF|ON|0|1

8 Enable/ disable the control descriptor word (CDW) feature.
*RST value: OFF

[:SOURce<ch>]:PDW:STATe OFF|ON|0|1

9 Enable/ disable the pulse descriptor word (PDW) feature.
*RST value: OFF

FCP Connector

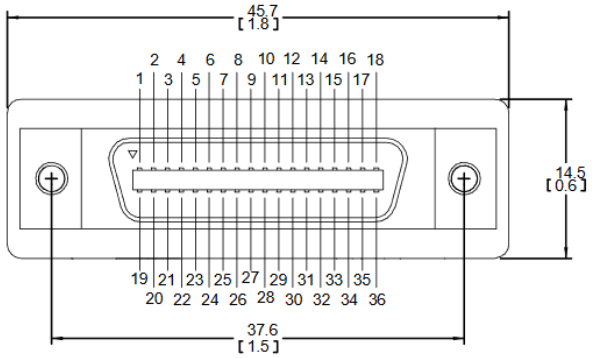
36 Pin MDR Connector

FCP Connector Counterpart Suggestion

- Required Connector: 36-pin mini-D male.
- Suggested Part: Connector Plug MDR 36 Pin (CONN PLUG 36POS STR SLDR CUP)
  3M part number: 10136-3000PE
- Cable Assembly: Requires additional connector back shell and shielded cable with 18 twisted pairs.

Pin Mapping on Connector

Pin		Signal	Pin		Signal
P	N	Name	P	N	Name
1	19	Data 0	10	28	Data 9
2	20	Data 1	11	29	Data 10
3	21	Data 2	12	30	Data 11
4	22	Data 3	13	31	Data 12
5	23	Data 4	14	32	Data 13
6	24	Data 5	15	33	Data 14
7	25	Data 6	16	34	Data 15
8	26	Data 7	17	35	Data valid
9	27	Data 8	18	36	Clock



36-pin mini-D male connector with FCP pin numbers.

Related Documentation

[1] Data Sheet APVSG
https://www.anapico.com/downloads/catalog-and-data-sheets/

[2] AnaPico Programmer's Manual for Signal Generators
https://www.anapico.com/downloads/manuals/

[3] AN6003 APVSG – Memory Segmentation
https://www.anapico.com/downloads/application-notes-and-videos/

[4] AN6008 APVSG – Pulse Descriptor Word
https://www.anapico.com/downloads/application-notes-and-videos/

[5] AN6009 APVSG – Control Descriptor Word
https://www.anapico.com/downloads/application-notes-and-videos/